WHAT IS CLAIMED IS:

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1. A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising the steps of:

simultaneously forming the oxide film on the floating gate of the said non-volatile memory cell transistor and a gate insulating film of the MOS transistor in a single thermal oxidation step.

2. A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising the steps of:

forming a silicon (Si) layer on the semiconductor substrate;

removing said Si layer on a region of said MOS transistor gate where a gate insulating film is to be formed;

forming an oxidation-resistant film on a region of said semiconductor substrate except the regions where the control gate of said non-volatile memory cell transistor is to be formed and where the gate insulating film of said MOS transistor is to be formed;

forming the oxide film by thermal oxidation on the region where the floating gate is to be formed; and

removing the remaining oxidation-resistant film,

whereby the oxide film on the floating gate of the said non-volatile memory cell transistor and the gate insulating film of said MOS transistor are simultaneously formed.

3. A method of manufacturing a semiconductor device according to claim 2, wherein said oxidation-resistant film is a silicon nitride film.

4. A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, comprising the steps of:

forming a first silicon (Si) layer on the semiconductor substrate;

selectively etching said first Si layer formed on a region where the gate insulating film of said MOS transistor is to be formed, thereby removing it;

covering an entire surface of the semiconductor substrate, inclusive of a side of said first Si layer exposed by the selective etching, with an oxidation-resistant film;

selectively removing said oxidation-resistant film on a

region where the gate insulating film of said MOS transistor is to be formed and selectively removing said oxidation-resistant film on a region where the floating gate of said non-volatile memory transistor is to be formed;

forming the oxide film by thermal oxidation on the region where said floating gate is to be formed and forming the gate insulating film on a region where said MOS transistor is to be formed;

removing the remaining oxidation-resistant film;

removing the remaining first Si layer using said oxide film as a mask, thereby forming the floating gate of said non-volatile memory cell transistor;

forming a tunneling insulating film of said non-volatile memory cell on the entire surface of the semiconductor substrate inclusive of the surface of the gate insulating film on the region where said MOS transistor is to be formed;

forming a second Si layer on the entire surface of said semiconductor substrate; and

selectively etching said second Si layer so that the control gate of said non-volatile memory cell and the gate of said MOS transistor are simultaneously formed.

5. A method of manufacturing a semiconductor device according to claim 4, further comprising the step of selectively removing said tunneling insulating film formed on the gate

insulating film on the region where said MOS transistor is to be formed.

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6. A method of manufacturing a semiconductor device according to claim 4 or 5, wherein said oxidation-resistant film is a silicon nitride film.

7. A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising the steps of:

forming a first silicon (Si) layer on the semiconductor substrate;

forming an oxidation-resistant oxide film on said first Si layer;

selectively removing the oxidation-resistant film on a region where said floating gate is to be formed;

selectively etching said first Si layer of said MOS transistor on a region where a gate insulating film is to be formed, thereby removing it;

forming the oxide film by thermal oxidation on the region where the floating gate is to be formed, the gate insulating film on the region where said MOS transistor is to be formed and an oxide film piece on the side of said first Si layer;

removing the remaining oxidation-resistant film;

removing said remaining first Si layer using said oxide film as a mask, thereby forming the floating gate of said non-volatile memory cell transistor;

forming a tunneling insulating film of said non-volatile memory cell on the entire surface of the semiconductor substrate inclusive of the surface of the gate insulating film on the region where said MOS transistor is to be formed;

forming a second Si layer on the entire surface of said semiconductor substrate; and

selectively etching said second Si layer so that the control gate of said non-volatile memory cell and the gate of said MOS transistor are simultaneously formed.

8. A method of manufacturing a semiconductor device according to claim 7, wherein a gate of said MOS transistor is formed to cover said oxide film piece.

9. A method of manufacturing a semiconductor device according to claim 7, further comprising the step of selectively removing said tunneling insulating film formed on the gate insulating film on the region where said MOS transistor is to be formed.

10. A method of manufacturing a semiconductor device

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according to claim 7, 8 or 9, wherein said oxidation-resistant film is a silicon nitride film.